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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/606,970	06/25/2003	Tong Tee Tan	70010721-2	6461

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AGILENT TECHNOLOGIES, INC.
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EXAMINER	
SIDDIQUI, SAQIB JAVAID	

ART UNIT	PAPER NUMBER
2138	

DATE MAILED: 11/01/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/606,970	TAN, TONG TEE	
	Examiner	Art Unit	
	Saqib J. Siddiqui	2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 June 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-22* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *06/25/2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☒ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *10/14/2003*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Priority

Acknowledgment is made of applicant's claim for foreign priority under 35 U.S.C. 119(a)-(d). The certified copy has been filed in parent Application No. 200203823-0, filed on June 25, 2002.

Oath/Declaration

The Oath filed June 25, 2003 complies with all the requirements set fort in MPEP 602 and therefore is accepted.

Drawings

The filed drawings are accepted.

Specification

The disclosure is objected to because of the following informalities:

(1) Field of the Invention: A statement of the field of art to which the invention pertains. This statement may include a paraphrasing of the applicable U.S. patent classification definitions of the subject matter of the claimed invention. This item may also be titled "Technical Field."

Field of the Invention has not been included. Appropriate correction is required.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-6, 8-11, 13-18, and 20-22 are rejected under 35 U.S.C. 102(b) as being fully anticipated by Gilley US 6,215,876 B1.

As per claim 1:

Gilley teaches a bit error detection circuit comprising a predictor circuit (Figure 4 # 60, column 6, lines 43-46) that uses a plurality of bits of a bit sequence to predict a next bit in the sequence, a comparator circuit (Figure 4 # 62, column 6, lines 46-49) that compares an actual next bit in the sequence with the predicted next bit to determine whether there is any error in the actual next bit and a correction circuit (Figure 4 # 78, column 7, lines 1-5) that corrects any error in the actual next bit to provide a corrected actual next bit.

As per claim 2:

Gilley teaches a bit error detection circuit wherein the correction circuit comprises a circuit element that replaces the actual next bit (Figure 4 # 74, columns 6-7, lines 66-3) with the corrected actual next bit in the plurality of bits.

As per claim 3:

Gilley teaches a bit error detection circuit wherein the bit sequence comprises a pseudo-random bit sequence (columns 5-6, lines 66-5) and the predictor circuit predicts the next bit by comparing two of the bits of the sequence (column 6, lines 26-45).

As per claim 4:

Gilley teaches a bit error detection circuit further comprising a trigger circuit that activates the correction circuit when the predictor circuit contains a plurality of bit in which no erroneous bits have been detected (Figure 4 # 68, columns 6, lines 46-57).

As per claim 5:

Gilley teaches a bit error detection circuit wherein the trigger circuit activates the correction circuit when no erroneous bits have been observed (columns 6, lines 50-51) during a predefined interval.

As per claim 6:

Gilley teaches a bit error detection circuit wherein the predefined interval is defined in terms of a quantity of bits (Figure 4 # 64, columns 6, lines 46-49).

As per claim 8:

Gilley teaches a bit error detection circuit comprising a shift register that receives N bits of a pseudo-random bit sequence (Figure 2 # 56, column 6, lines 43-45), a first logic element that receives output signals from two stages of the shift register and provides a signal indicative of a predicted *(N+1)-th* bit (Figure 4 # 60, column 6, lines 43-45), a second logic element that receives the signal indicative of the predicted *(N+1)-th* bit and a signal indicative of and actual *(N+1)-th* bit and provides and output signal indicative of any error in the actual *(N+1)-th* bit (Figure 4 # 62, column 6, lines 46-49), and a third logic element that receives the output signal and corrects the actual *(N+1)-th* bit according to the output signal (Figure 4 # 72, column 6, lines 58-65) as the *(N+1)-th* bit propagates through the shift register.

As per claim 9:

Gilley teaches a bit error detection circuit wherein the third logic element receives the actual *(N+1)-th* bit from one of the shift register stages (Figure 4 # 66, column 6, lines 58-65), corrects said bit according to the output signal (Figure 4 # 72, column 6, lines 58-60), and inserts said bit as corrected into another one of the shift register stages in place of the actual *(N+1)-th* bit (Figure 4 # 74, columns 6-7, lines 66-69).

As per claim 10:

Gilley teaches a bit error detection circuit further comprising a trigger circuit (Figure 4 # 68, column 6, lines 46-57) that activates the third logic element when the shift registers contain a bit sequence in which no erroneous bits have been detected.

As per claim 11:

Gilley teaches a bit error detection circuit wherein the trigger circuit comprises a logic circuit that receives the output signal and provides an enabling signal if no error is indicated (Figure 4 # 70, column 6, lines 49-52) while a predefined number of bits propagates through the shift register.

As per claim 13:

Gilley teaches a bit error detection circuit wherein the trigger circuit prevents the third logic element from correcting any bits until the shift register contains a bit sequence in which no error has been detected (Figure 4 # 66, column 6, lines 49-57).

As per claim 14:

Gilley teaches a method of detecting errors in a bit sequence comprising predicting a next bit of a bit sequence according to a plurality of previous bits of the

sequence (Figure 4 # 60, column 6, lines 43-45), comparing the predicted bit with an actual next bit (Figure 4 # 62, column 6, lines 46-49), and if the comparison indicates a difference between the predicted and actual next bits (Figure 4 # 72 & 76, column 6, lines 58-65), providing an error signal (Figure 4 # 78, column 7, lines 1-5) and correcting the actual next bit (Figure 4 # 74 & 76, columns 6-7, lines 66-5).

As per claim 15:

Gilley teaches a method of detecting errors in a bit sequence wherein correcting the actual next bit comprises replacing the actual next bit with the corrected actual next bit in the bit sequence (Figure 4 # 74, columns 6-7, lines 66-2).

As per claim 16:

Gilley teaches method of detecting errors in a bit sequence wherein the bit sequence comprises a pseudo-random bit sequence (columns 5-6, lines 66-5).

As per claim 17:

Gilley teaches a method of detecting errors in a bit sequence further comprising suppressing any correction of the actual next bit until no error has been detected in a plurality of bits in the sequence (Figure 4 # 66, column 6, lines 49-57).

As per claim 18:

Gilley teaches a method of detecting errors in a bit sequence further comprising determining whether any bit errors are detected during a predefined interval (Figure 4 # 64, column 6, lines 46-49).

As per claim 20:

Gilley teaches a method of detecting errors in a bit sequence further comprising counting a predefined number of bits as they propagate through a circuit element to determine when the predefined interval has elapsed (Figure 4 # 62, column 6, lines 45-48).

As per claim 21:

Gilley teaches a bit error detector comprising an actual next bit input that receives a plurality of bits of a bit sequence (Figure 2 # 56, column 6, lines 43-45), a predictor (Figure 4 # 60, column 6, lines 43-45) coupled to the input and having a predicted next bit output, a comparator coupled to the predicted next bit output and to the actual next bit input (Figure 4 # 62, column 6, lines 45-48), the comparator having an error signal output (Figure 4 # 64, column 6, lines 47-49), and a corrector coupled to the error signal output (Figure 4 # 72, column 6, lines 58-65) and having a corrected actual next bit output (Figure 4 # 74, columns 6-7, lines 66-1).

As per claim 22:

Gilley teaches a bit error detector wherein the predictor comprises a predictor circuit for receiving the plurality of bits (Figure 4 # 60, column 6, lines 43-45), for determining a predicted next bit from at least some of the plurality of its, and for providing the predicted next bit at the predicted next bit output (Figure 4 # 62, column 6, lines 46-48), the comparator comprises a comparator circuit for receiving the predicted next bit and the actual next bit (Figure 4 # 62, column 6, lines 45-50), for comparing the predicted next bit and the actual next bit, and for providing an error signal at the error signal output (column 6, lines 52-57) when a difference is detected between the

predicted next bit and the actual next bit, and the corrector comprises a correction circuit for receiving the error signal (Figure 4 # 72, column 6, lines 58-60) producing a corrected actual next bit, and providing the corrected actual next bit at the corrected actual next output (columns 6-7, lines 66-5) .

Claim Rejections - 35 USC § 103

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

Claims 7, 12, and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gilley US 6,215,876 B1, and further in view of Yoshimura et al. US 5,123,020.

As per claim 7:

Gilley substantially teaches a bit error detection circuit comprising a predictor circuit (Figure 4 # 60, column 6, lines 43-46) that uses a plurality of bits of a bit sequence to predict a next bit in the sequence, a comparator circuit (Figure 4 # 62, column 6, lines 46-49) that compares an actual next bit in the sequence with the predicted next bit to determine whether there is any error in the actual next bit, a correction circuit (Figure 4 # 78, column 7, lines 1-5) that corrects any error in the actual next bit to provide a corrected actual next bit, a trigger circuit that activates the

correction circuit when the predictor circuit contains a plurality of bit in which no erroneous bits have been detected (Figure 4 # 68, columns 6, lines 46-57), wherein the trigger circuit activates the correction circuit when no erroneous bits have been observed (columns 6, lines 50-51) during a predefined interval.

Gilley does not explicitly teach the predefined interval to be defined in terms of an interval of time.

However, Yoshimura et al. in an analogous art, teaches an error detection circuit wherein the predefined interval is defined in terms of an interval of time (columns 7-8, lines 61-6). Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to use define the interval in terms of time within the error detection circuit of Gilley. This modification would have been obvious to one of ordinary skill in the art because one of ordinary skill in the art would have recognized that using the time interval would have allowed activating the circuit manually and would make the reset process more predictable.

As per claim 12:

Gilley substantially teaches a bit error detection circuit comprising a shift register that receives N bits of a pseudo-random bit sequence (Figure 2 # 56, column 6, lines 43-45), a first logic element that receives output signals from two stages of the shift register and provides a signal indicative of a predicted *(N+1)-th* bit (Figure 4 # 60, column 6, lines 43-45), a second logic element that receives the signal indicative of the predicted *(N+1)-th* bit and a signal indicative of and actual *(N+1)-th* bit and provides and output signal indicative of any error in the actual *(N+1)-th* bit (Figure 4 # 62, column 6,

lines 46-49), a third logic element that receives the output signal and corrects the actual *(N+1)-th* bit according to the output signal (Figure 4 # 72, column 6, lines 58-65) as the *(N+1)-th* bit propagates through the shift register, further comprising a trigger circuit (Figure 4 # 68, columns 6, lines 46-57) that activates the third logic element when the shift registers contain a bit sequence in which no erroneous bits have been detected.

Gilley does not explicitly teach the trigger circuit comprising a timer that provides an enabling signal if no error is indicated during a predefined time interval.

However, Yoshimura et al. in an analogous art, teaches an error detection circuit wherein the trigger circuit comprises a timer that provides an enabling signal if no error is indicated during a predefined time interval (columns 7-8, lines 61-6). Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to use define the interval in terms of time within the error detection circuit of Gilley. This modification would have been obvious to one of ordinary skill in the art because one of ordinary skill in the art would have recognized that using the time interval would have allowed activating the circuit manually and would make the reset process more predictable.

As per claim 19:

Gilley substantially teaches a method of detecting errors in a bit sequence comprising predicting a next bit of a bit sequence according to a plurality of previous bits of the sequence (Figure 4 # 60, column 6, lines 43-45), comparing the predicted bit with an actual next bit (Figure 4 # 62, column 6, lines 46-49), and if the comparison indicates a difference between the predicted and actual next bits (Figure 4 # 72 & 76, column 6,

lines 58-65), providing an error signal (Figure 4 # 78, column 7, lines 1-5), correcting the actual next bit (Figure 4 # 74 & 76, columns 6-7, lines 66-5), and further comprising determining whether any bit errors are detected during a predefined interval (Figure 4 # 64, column 6, lines 46-49).

Gilley does not explicitly teach the measuring a period of time to determine when the predefined interval has elapsed.

However, Yoshimura et al. in an analogous art, teaches an error detection circuit wherein the further comprising measuring a period of time to determine when the predefined interval has elapsed (columns 7-8, lines 59-6). Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to use define the interval in terms of time within the error detection circuit of Gilley. This modification would have been obvious to one of ordinary skill in the art because one of ordinary skill in the art would have recognized that using the time interval would have allowed activating the circuit manually and would make the reset process more predictable.

Related Art

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Additional pertinent prior arts, US 6002714 A, US 5606322 A, US 20030005383 A1, US 4646312 A and, US 5043990 A mention the same pattern of error detection circuit comprising predictor, comparator and correction aspects are included herein for Applicant's review.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Saqib J. Siddiqui whose telephone number is (571) 272-6553. The examiner can normally be reached on 8:00 to 4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on (571) 272-3819. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Saqib Siddiqui
Art Unit 2133
10/14/2005

GUY LAMARRE
PRIMARY EXAMINER